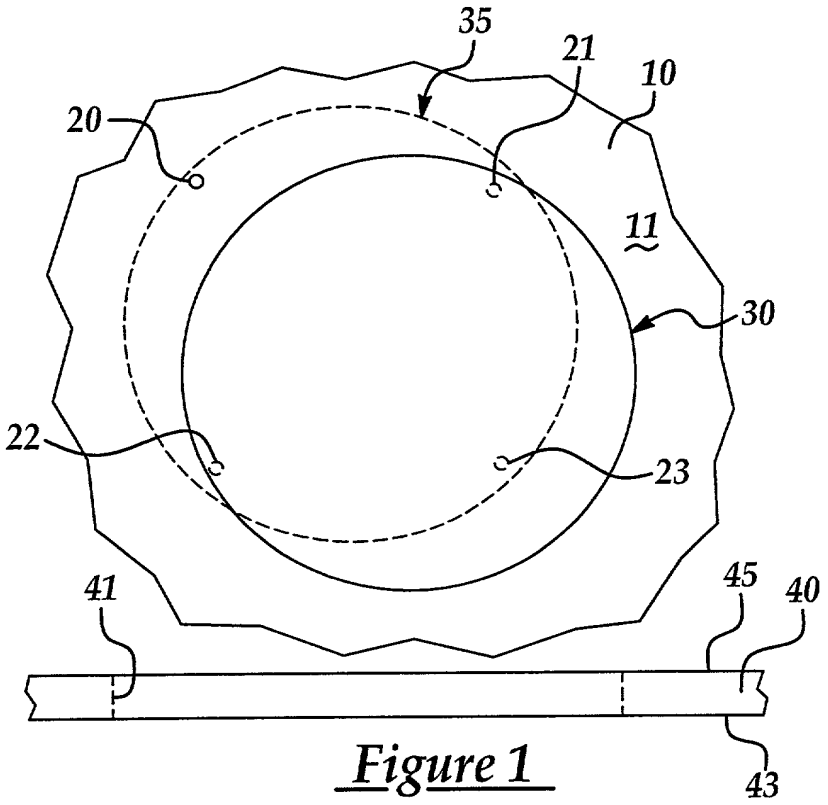

Figure 1

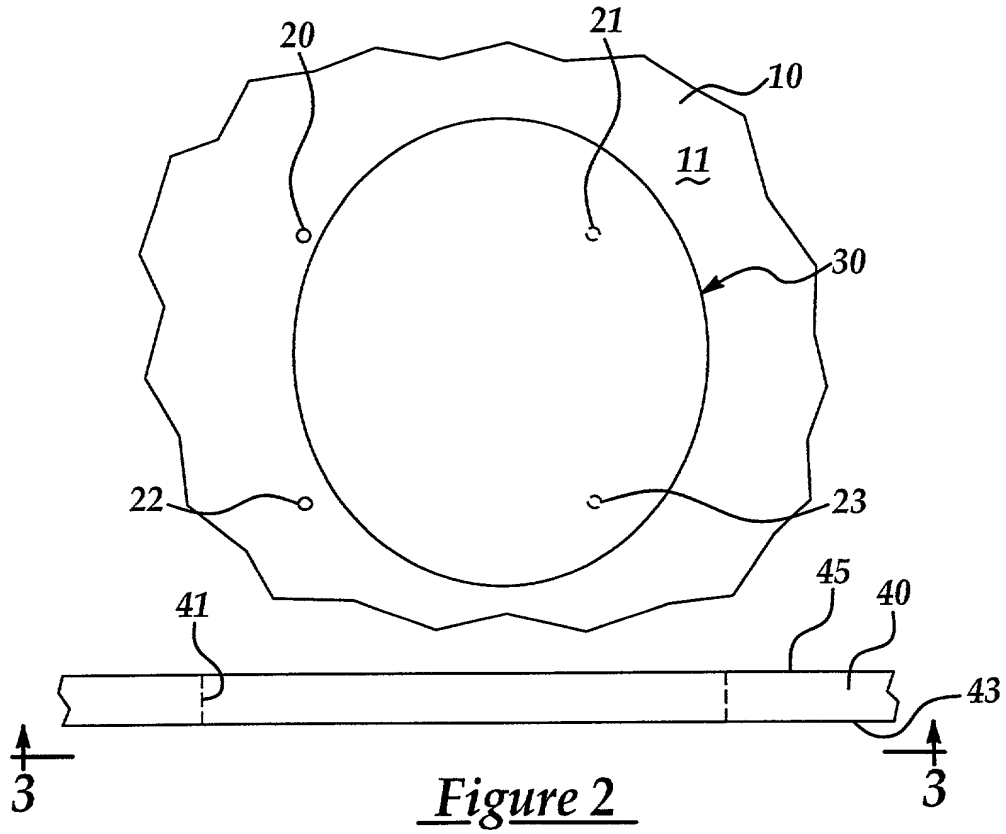

Figure 2

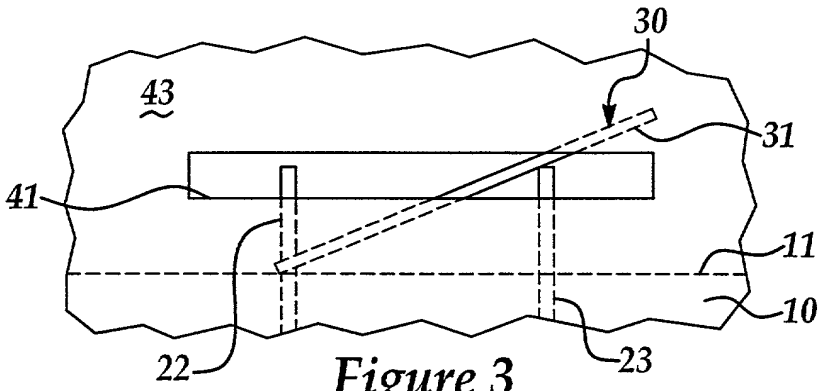

Figure 3

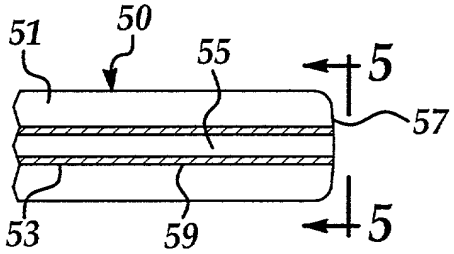

Figure 4

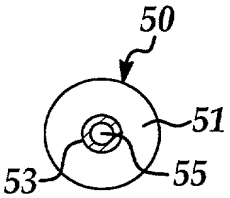

Figure 5

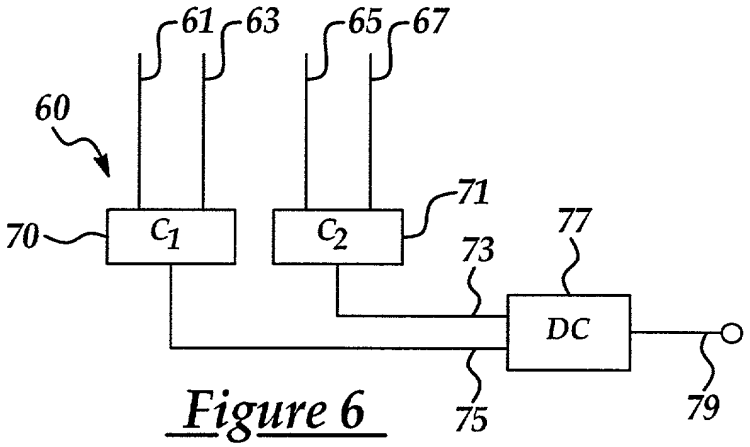

Figure 6

WAFER STATUS	P1	P2	P3	P4	FAULT
MISSING/BROKEN	0	0	0	0	1
MISPOSITIONED	0	X	X	X	1
MISPOSITIONED	X	0	X	X	1
MISPOSITIONED	X	X	0	X	1
MISPOSITIONED	X	X	X	0	1
PROPER	1	1	1	1	0

Figure 7

WAFER STATUS	C1	C2	DC
BROKEN/MISSING	0	0	1
MISPOSITIONED	0	1	1
	1	0	1
PROPER	1	1	0

Figure 8

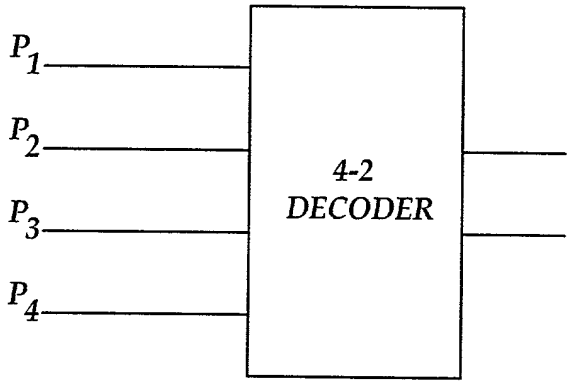

Figure 9

WAFER STATUS	P1	P2	P3	P4	FAULT
MISSING/BROKEN	0	0	0	0	1/1
MISPOSITIONED (OFF 2 PINS)	0	0	X	X	1/0
MISPOSITIONED (OFF 1 PIN)	0	1	1	1	0/1
MISPOSITIONED (OFF 2 PINS)	X	0	0	X	1/0
MISPOSITIONED (OFF 1 PIN1)	1	0	1	1	0/1
MISPOSITIONED (OFF 2 PINS)	X	X	0	0	1/0
MISPOSITIONED (OFF 1 PIN)	1	1	0	1	0/1
MISPOSITIONED (OFF 2 PINS)	0	X	X	0	1/0
MISPOSITIONED (OFF 1 PIN)	1	1	1	0	0/1
PROPER	1	1	1	1	0/0

Figure 10